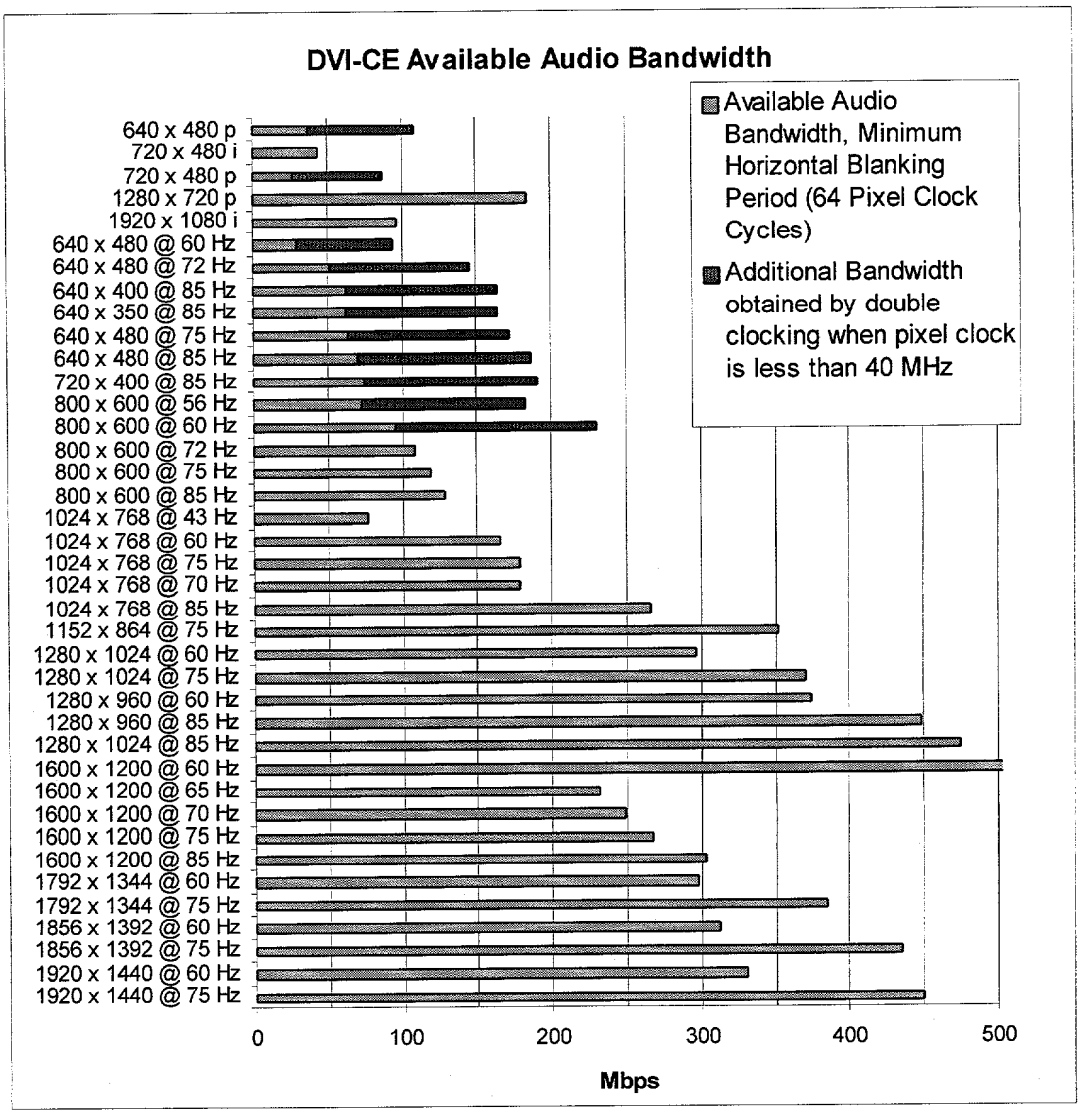

DVI-CE Available Audio Bandwidth
Available Audio Bandwidth, Minimum Horizontal Blanking Period (64 Pixel Clock Cycles)
Additional Bandwidth obtained by double clocking when pixel clock is less than 40 MHz
640 x 480 p
720 x 480 i
720 x 480 p
1280 x 720 p
1920 x 1080 i
640 x 480 @ 60 Hz
640 x 480 @ 72 Hz
640 x 400 @ 85 Hz
640 x 350 @ 85 Hz
640 x 480 @ 75 Hz
640 x 480 @ 85 Hz
720 x 400 @ 85 Hz
800 x 600 @ 56 Hz
800 x 600 @ 60 Hz
800 x 600 @ 72 Hz
800 x 600 @ 75 Hz
800 x 600 @ 85 Hz
1024 x 768 @ 43 Hz
1024 x 768 @ 60 Hz
1024 x 768 @ 75 Hz
1024 x 768 @ 70 Hz
1024 x 768 @ 85 Hz
1152 x 864 @ 75 Hz
1280 x 1024 @ 60 Hz
1280 x 1024 @ 75 Hz
1280 x 960 @ 60 Hz
1280 x 960 @ 85 Hz
1280 x 1024 @ 85 Hz
1600 x 1200 @ 60 Hz
1600 x 1200 @ 65 Hz
1600 x 1200 @ 70 Hz
1600 x 1200 @ 75 Hz
1600 x 1200 @ 85 Hz
1792 x 1344 @ 60 Hz
1792 x 1344 @ 75 Hz
1856 x 1392 @ 60 Hz
1856 x 1392 @ 75 Hz
1920 x 1440 @ 60 Hz
1920 x 1440 @ 75 Hz
0
100
200
300
400
500
Mbps

Fig. 1

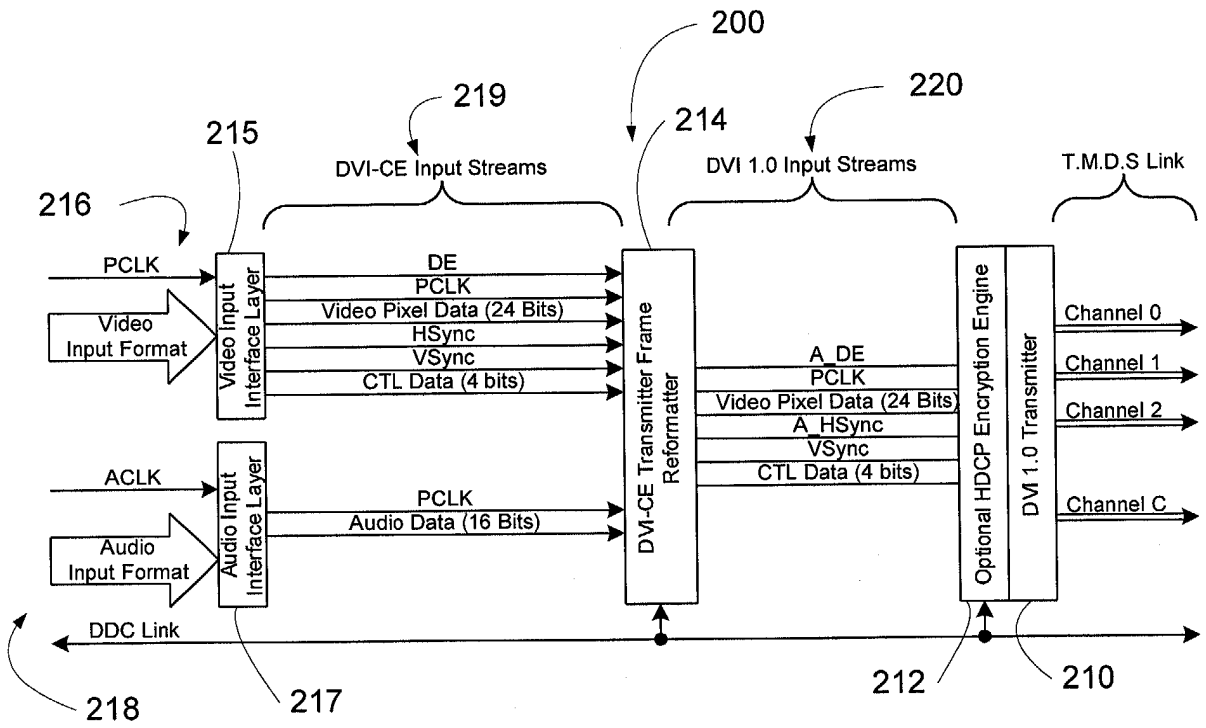

200
219
220
214
215
216
DVI-CE Input Streams
DVI 1.0 Input Streams
T.M.D.S Link
PCLK
Video Input Format
Video Input Interface Layer
DE
PCLK
Video Pixel Data (24 Bits)
HSync
VSync
CTL Data (4 bits)
ACLK
Audio Input Format
Audio Input Interface Layer
PCLK
Audio Data (16 Bits)
DVI-CE Transmitter Frame Reformatter
A_DE
PCLK
Video Pixel Data (24 Bits)
A_HSync
VSync
CTL Data (4 bits)
Optional HDCP Encryption Engine
DVI 1.0 Transmitter
Channel 0
Channel 1
Channel 2
Channel C
DDC Link
218
217
212
210

Fig. 2

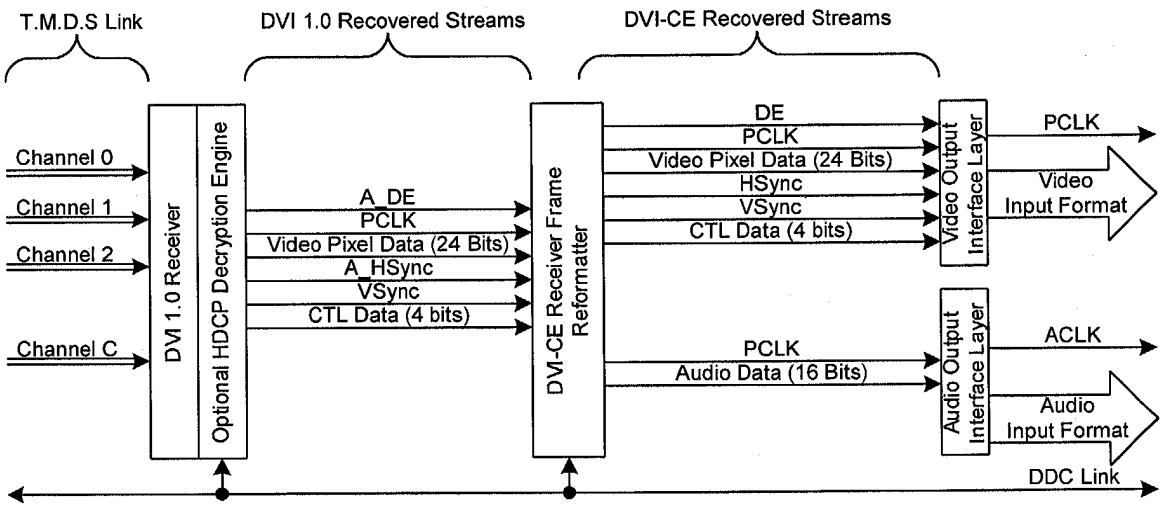

T.M.D.S Link
DVI 1.0 Recovered Streams
DVI-CE Recovered Streams
Channel 0
Channel 1
Channel 2
Channel C
DVI 1.0 Receiver
Optional HDCP Decryption Engine
A_DE
PCLK
Video Pixel Data (24 Bits)
A_HSync
VSync
CTL Data (4 bits)
DVI-CE Receiver Frame Reformatter
DE
PCLK
Video Pixel Data (24 Bits)
HSync
VSync
CTL Data (4 bits)
Video Output Interface Layer
PCLK
Video Input Format
PCLK
Audio Data (16 Bits)
Audio Output Interface Layer
ACLK
Audio Input Format
DDC Link

Fig. 3

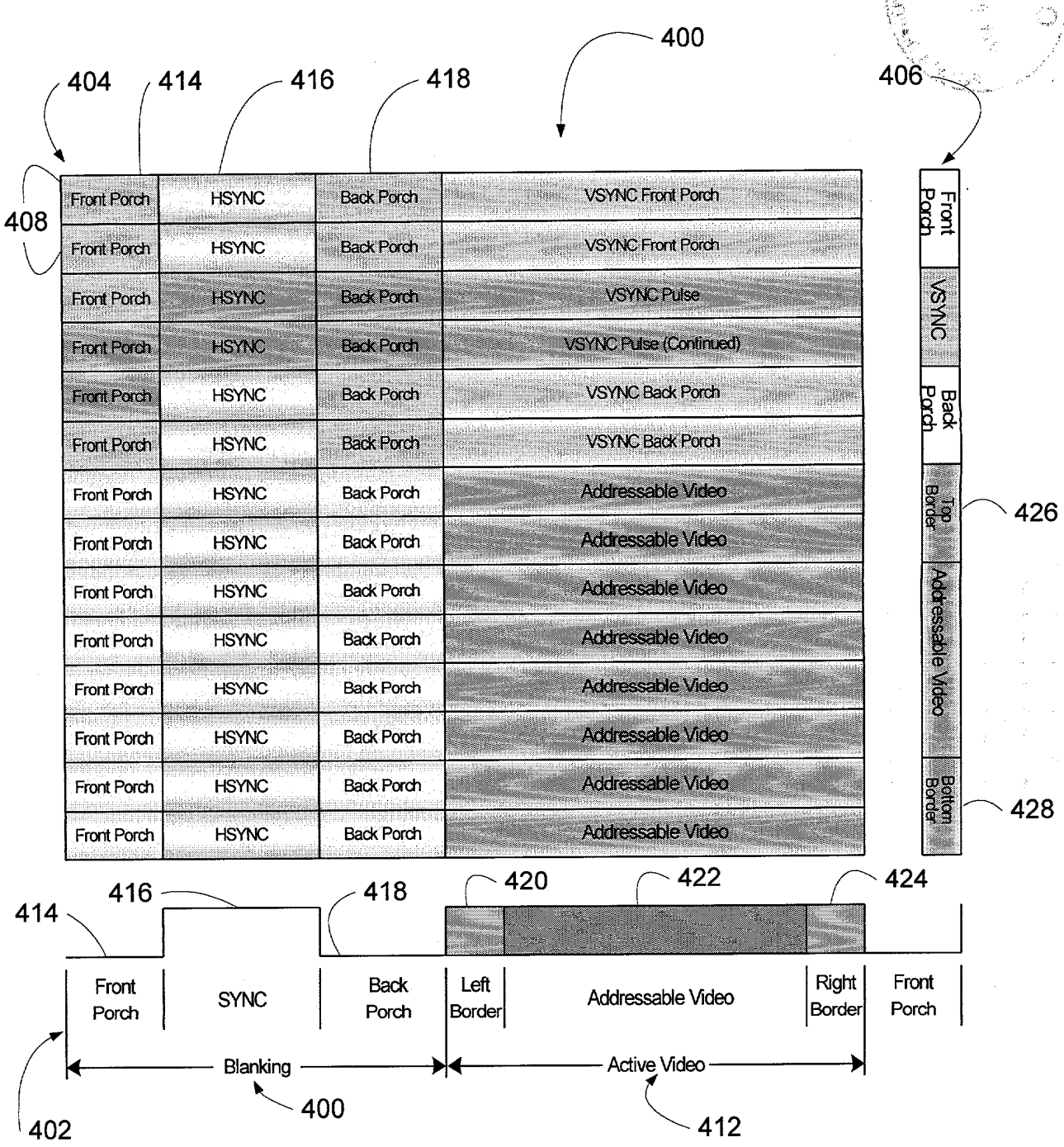

400
404
414
416
418
406
408
Front Porch
HSYNC
Back Porch
VSYNC Front Porch
VSYNC Pulse
VSYNC Pulse (Continued)
VSYNC Back Porch
Addressable Video
VSYNC
Top Border
Addressable Video
Bottom Border
426
428
420
422
424
Front Porch
SYNC
Back Porch
Left Border
Addressable Video
Right Border
Blanking
Active Video
402
412

Fig. 4

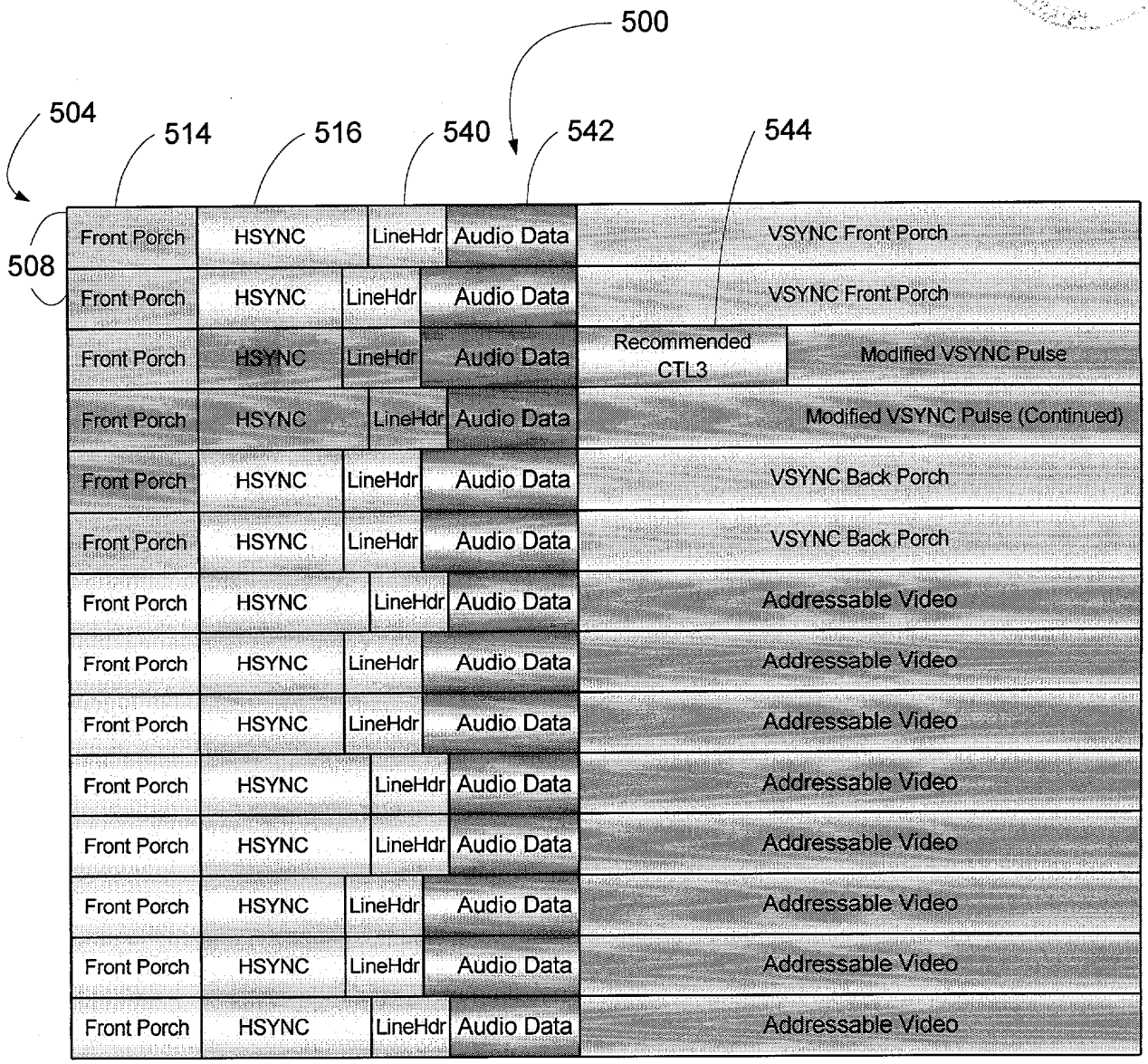

500
504
514
516
540
542
544
508
Front Porch
HSYNC
LineHdr
Audio Data
VSYNC Front Porch
VSYNC Front Porch
Recommended CTL3
Modified VSYNC Pulse
Modified VSYNC Pulse (Continued)
VSYNC Back Porch
VSYNC Back Porch
Addressable Video
Addressable Video
Addressable Video
Addressable Video
Addressable Video
Addressable Video
Addressable Video

Fig. 5

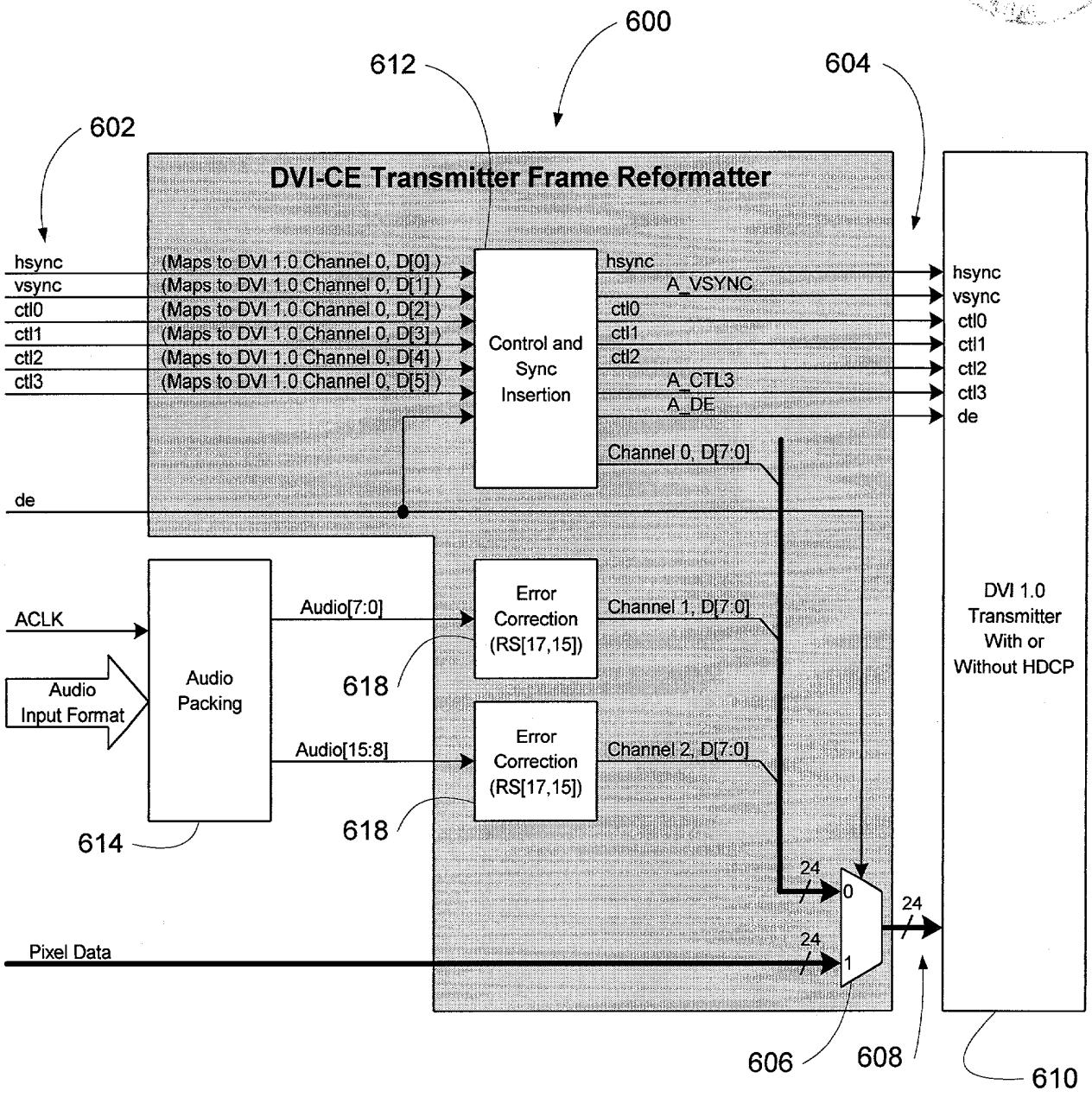

600
612
604
602
DVI-CE Transmitter Frame Reformatter
hsync
vsync
ctl0
ctl1
ctl2
ctl3
(Maps to DVI 1.0 Channel 0, D[0])
(Maps to DVI 1.0 Channel 0, D[1])
(Maps to DVI 1.0 Channel 0, D[2])
(Maps to DVI 1.0 Channel 0, D[3])
(Maps to DVI 1.0 Channel 0, D[4])
(Maps to DVI 1.0 Channel 0, D[5])
Control and Sync Insertion
hsync
A_VSYNC
ctl0
ctl1
ctl2
A_CTL3
A_DE
Channel 0, D[7:0]
de
ACLK
Audio Input Format
Audio Packing
Audio[7:0]
Audio[15:8]
Error Correction (RS[17,15])
Error Correction (RS[17,15])
Channel 1, D[7:0]
Channel 2, D[7:0]
618
618
614
24
24
24
0
1
Pixel Data
DVI 1.0 Transmitter With or Without HDCP
hsync
vsync
ctl0
ctl1
ctl2
ctl3
de
606
608
610

Fig. 6

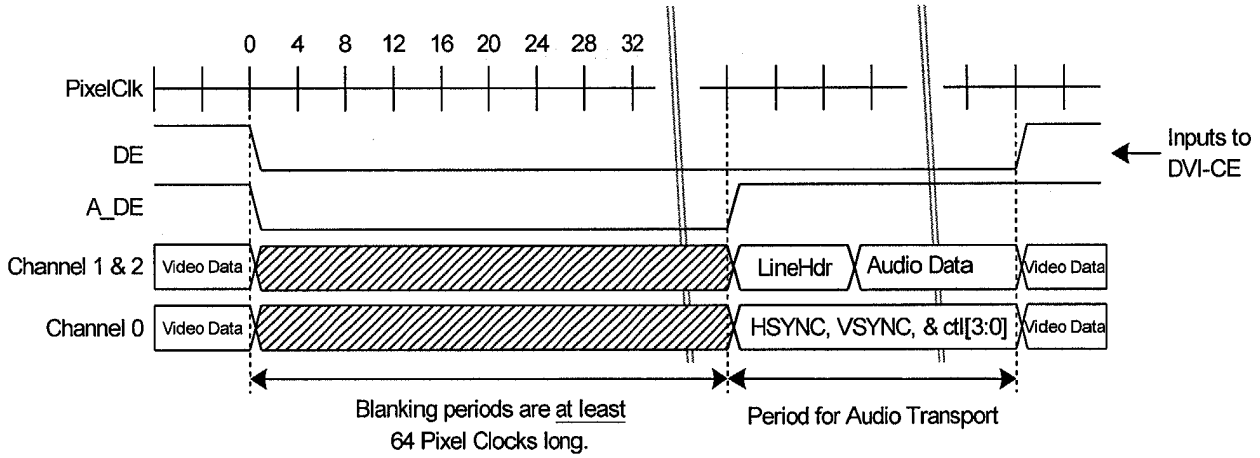


Fig. 7

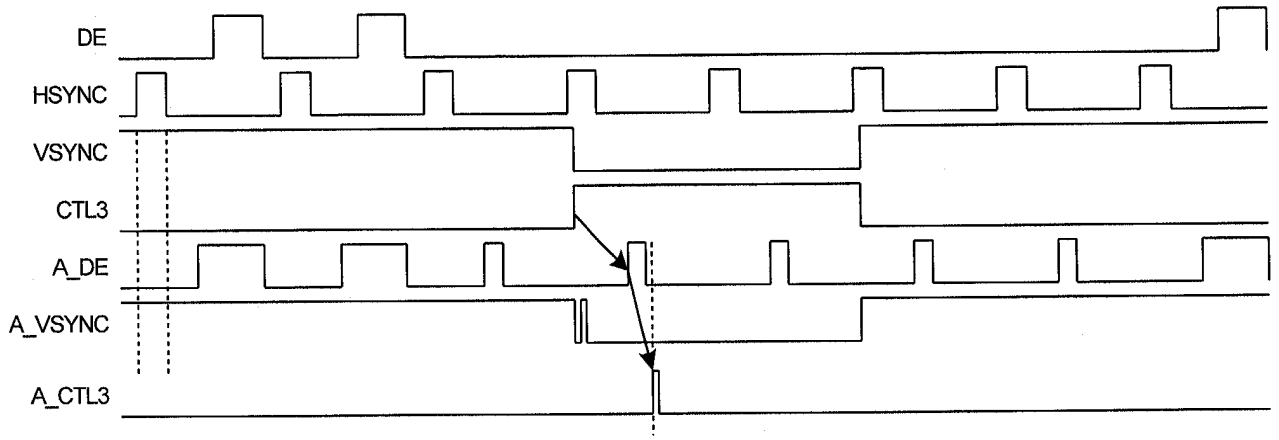


Fig. 8

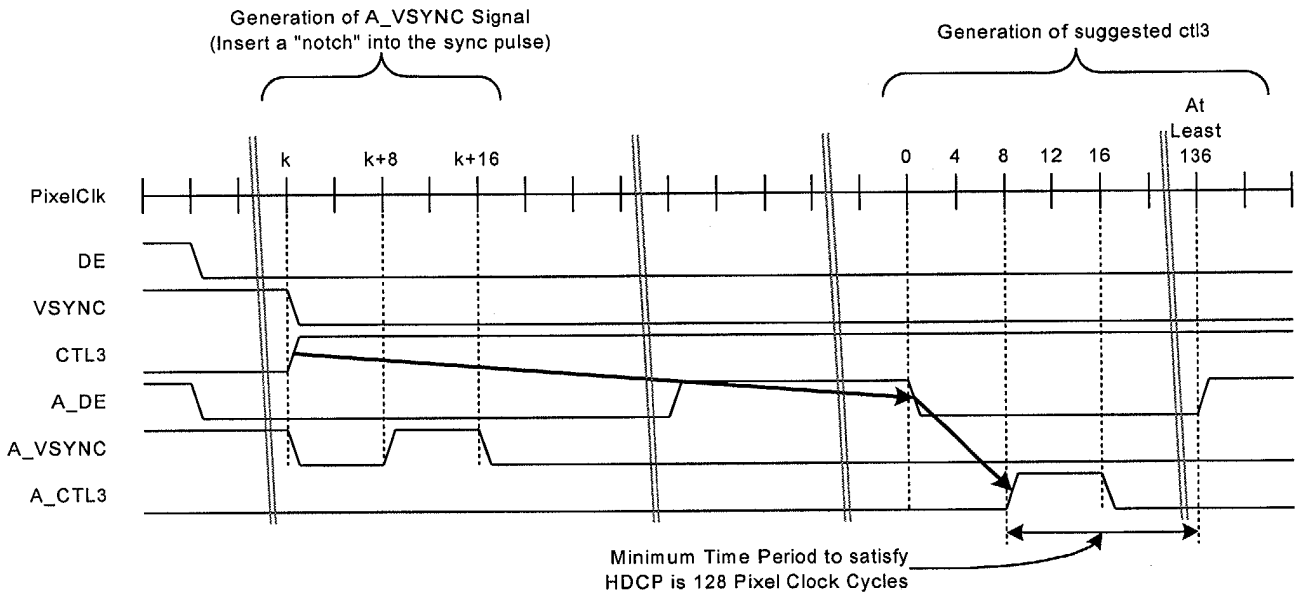

Generation of A_VSYNC Signal
(Insert a "notch" into the sync pulse)
Generation of suggested ctl3
At
Least
k
k+8
k+16
0
4
8
12
16
136
PixelClk
DE
VSYNC
CTL3
A_DE
A_VSYNC
A_CTL3
Minimum Time Period to satisfy
HDCP is 128 Pixel Clock Cycles

Fig. 9

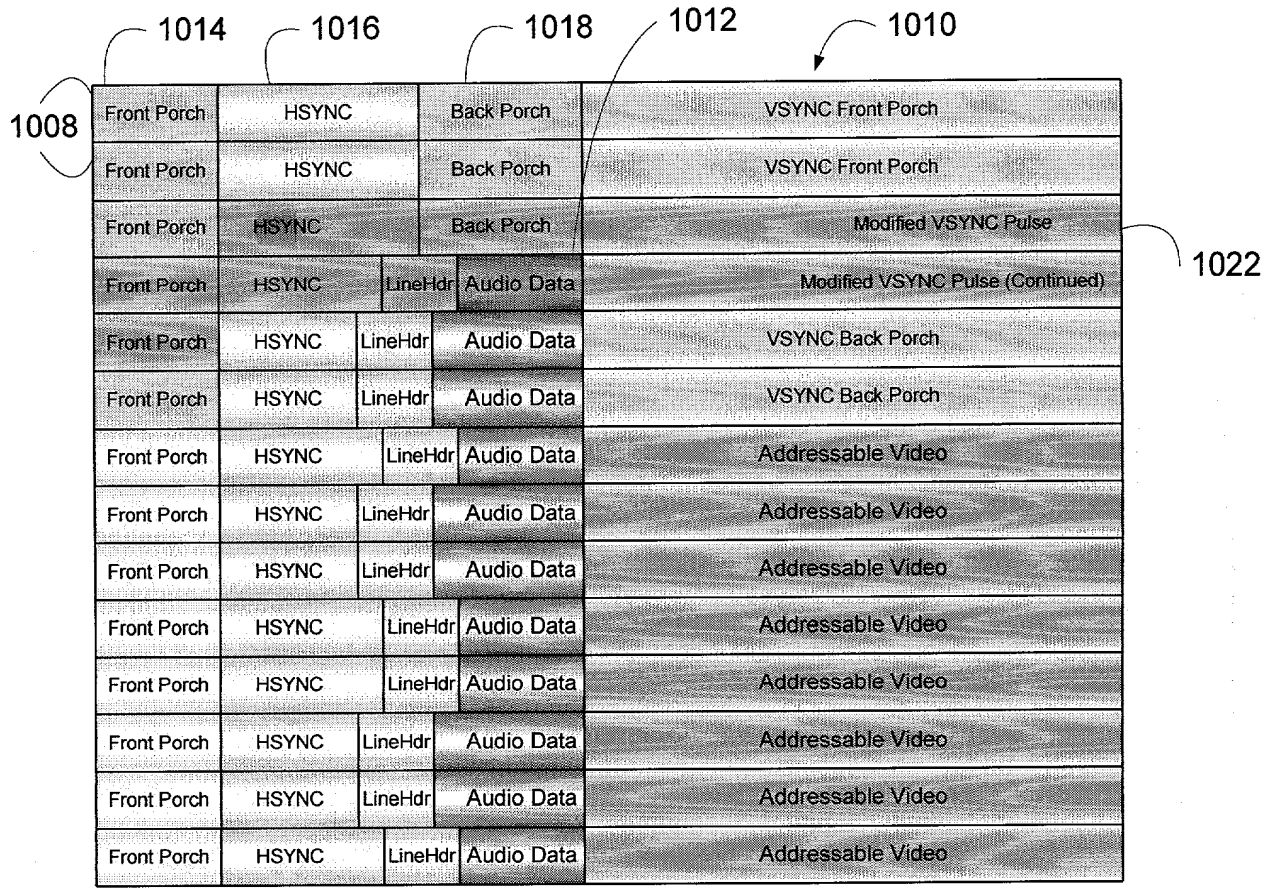

1014
1016
1018
1012
1010
1008
1022
Front Porch
HSYNC
Back Porch
VSYNC Front Porch
Front Porch
HSYNC
Back Porch
VSYNC Front Porch
Front Porch
HSYNC
Back Porch
Modified VSYNC Pulse
Front Porch
HSYNC
LineHdr
Audio Data
Modified VSYNC Pulse (Continued)
Front Porch
HSYNC
LineHdr
Audio Data
VSYNC Back Porch
Front Porch
HSYNC
LineHdr
Audio Data
VSYNC Back Porch
Front Porch
HSYNC
LineHdr
Audio Data
Addressable Video
Front Porch
HSYNC
LineHdr
Audio Data
Addressable Video
Front Porch
HSYNC
LineHdr
Audio Data
Addressable Video
Front Porch
HSYNC
LineHdr
Audio Data
Addressable Video
Front Porch
HSYNC
LineHdr
Audio Data
Addressable Video
Front Porch
HSYNC
LineHdr
Audio Data
Addressable Video
Front Porch
HSYNC
LineHdr
Audio Data
Addressable Video

Fig. 10

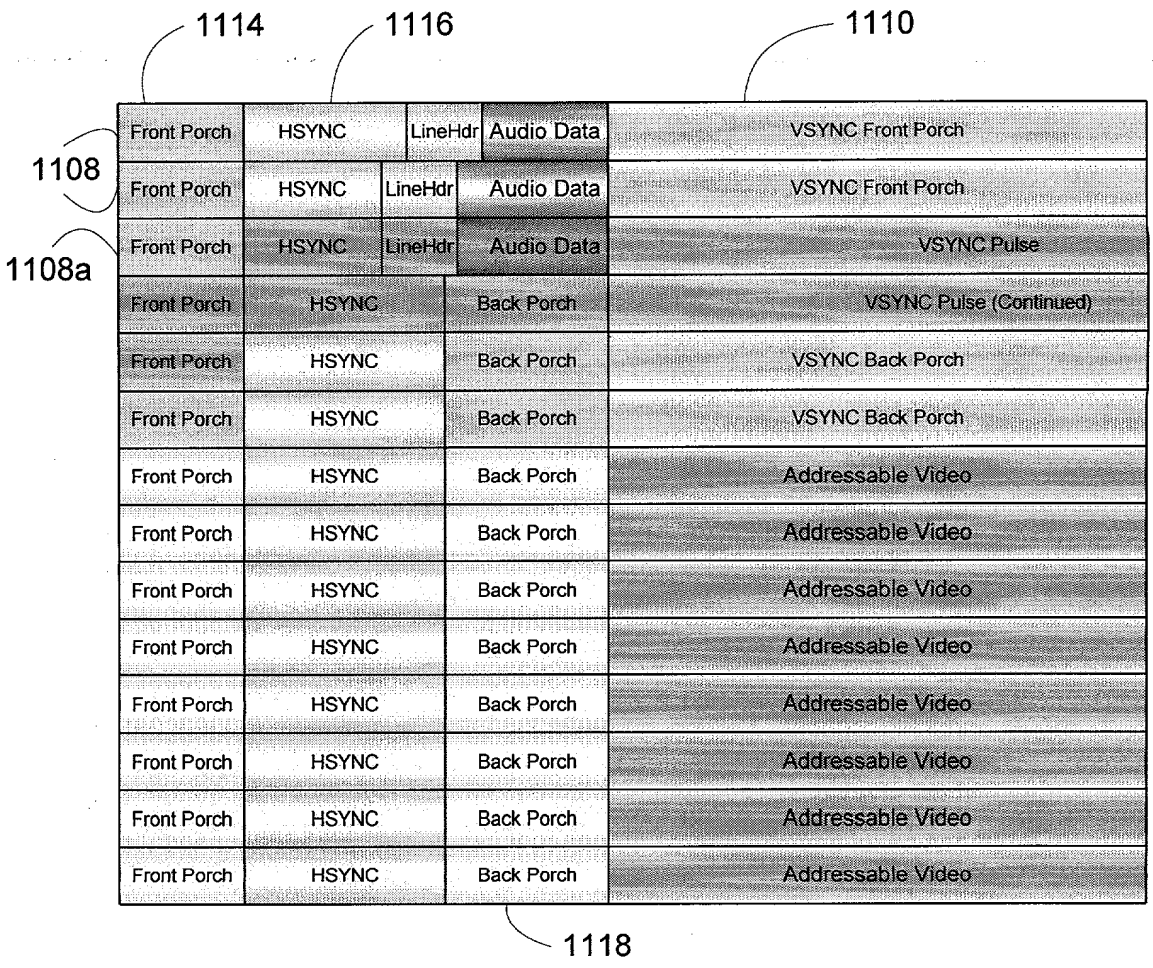

1114
1116
1110
1108
1108a
Front Porch
HSYNC
LineHdr
Audio Data
VSYNC Front Porch
VSYNC Pulse
VSYNC Pulse (Continued)
Back Porch
VSYNC Back Porch
Addressable Video
1118

Fig. 11

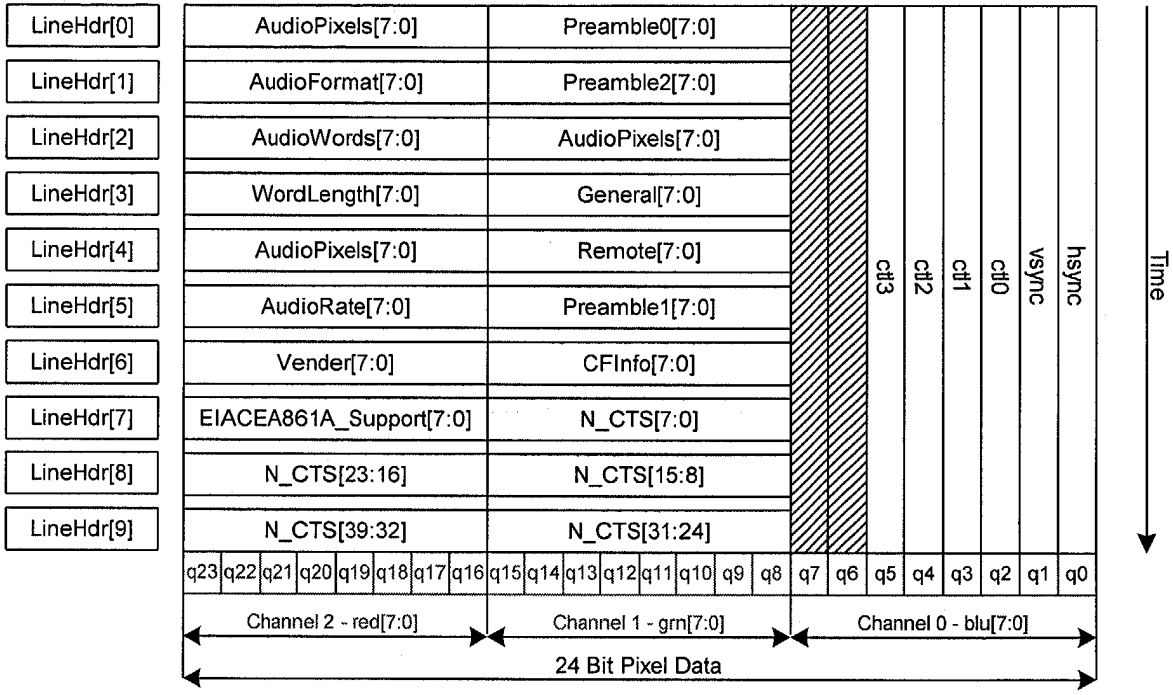


Fig. 12

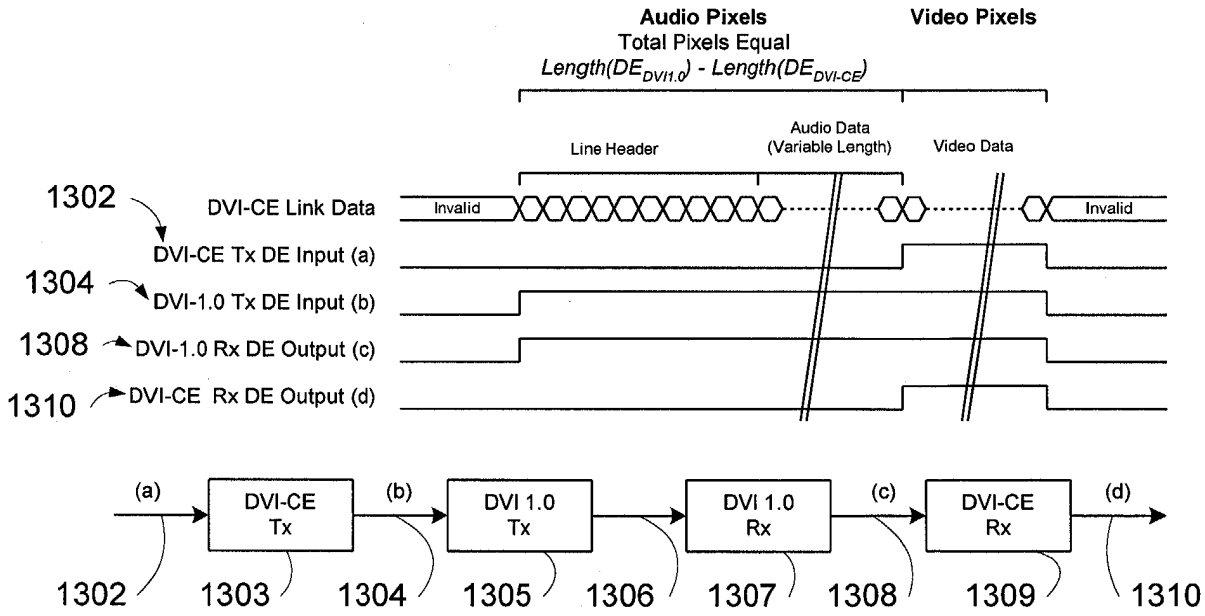
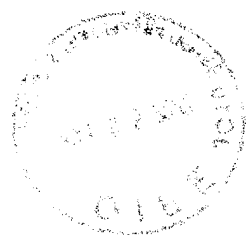

Audio Pixels
Total Pixels Equal
Length(DE_DVI1.0) - Length(DE_DVI-CE)
Video Pixels
Line Header
Audio Data
(Variable Length)
Video Data
1302
DVI-CE Link Data
Invalid
Invalid
DVI-CE Tx DE Input (a)
1304
DVI-1.0 Tx DE Input (b)
1308
DVI-1.0 Rx DE Output (c)
1310
DVI-CE Rx DE Output (d)
(a)
DVI-CE Tx
(b)
DVI 1.0 Tx
DVI 1.0 Rx
(c)
DVI-CE Rx
(d)
1302
1303
1304
1305
1306
1307
1308
1309
1310

Fig. 13



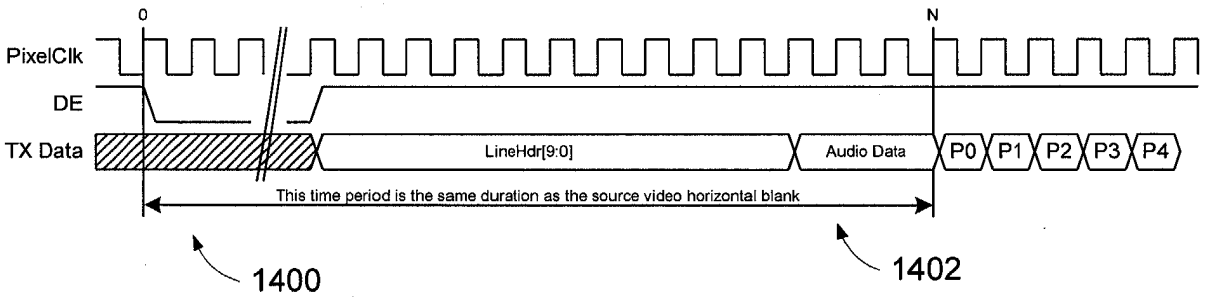

0
N
PixelClk
DE
TX Data
LineHdr[9:0]
Audio Data
P0
P1
P2
P3
P4
This time period is the same duration as the source video horizontal blank
1400
1402

Fig. 14

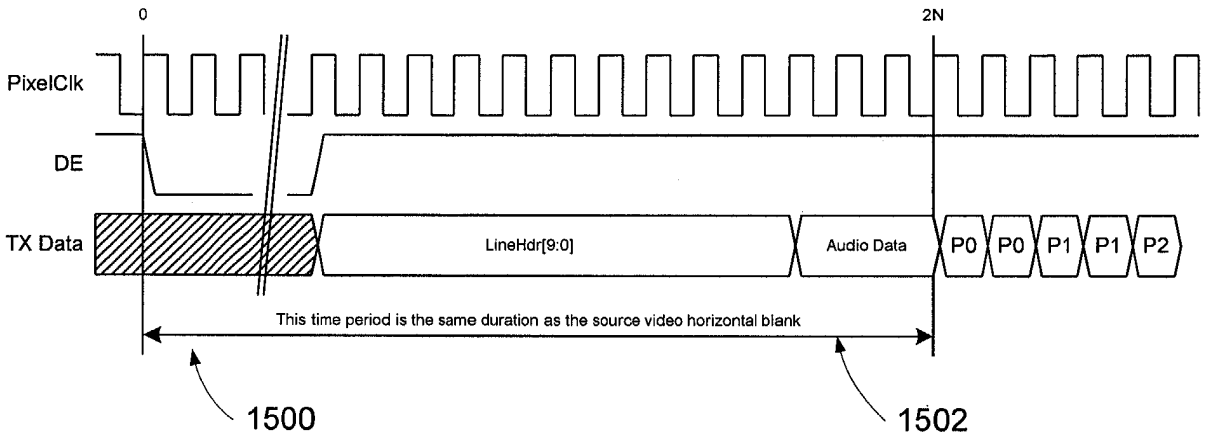

0
2N
PixelClk
DE
TX Data
LineHdr[9:0]
Audio Data
P0
P0
P1
P1
P2
This time period is the same duration as the source video horizontal blank
1500
1502

Fig. 15

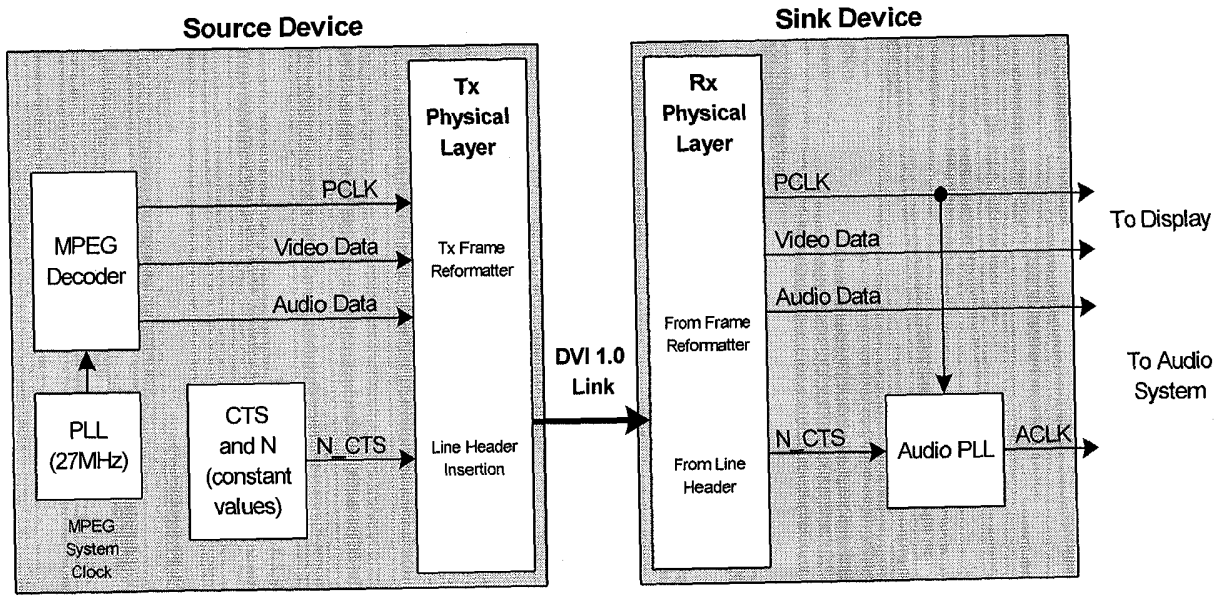


Fig. 16

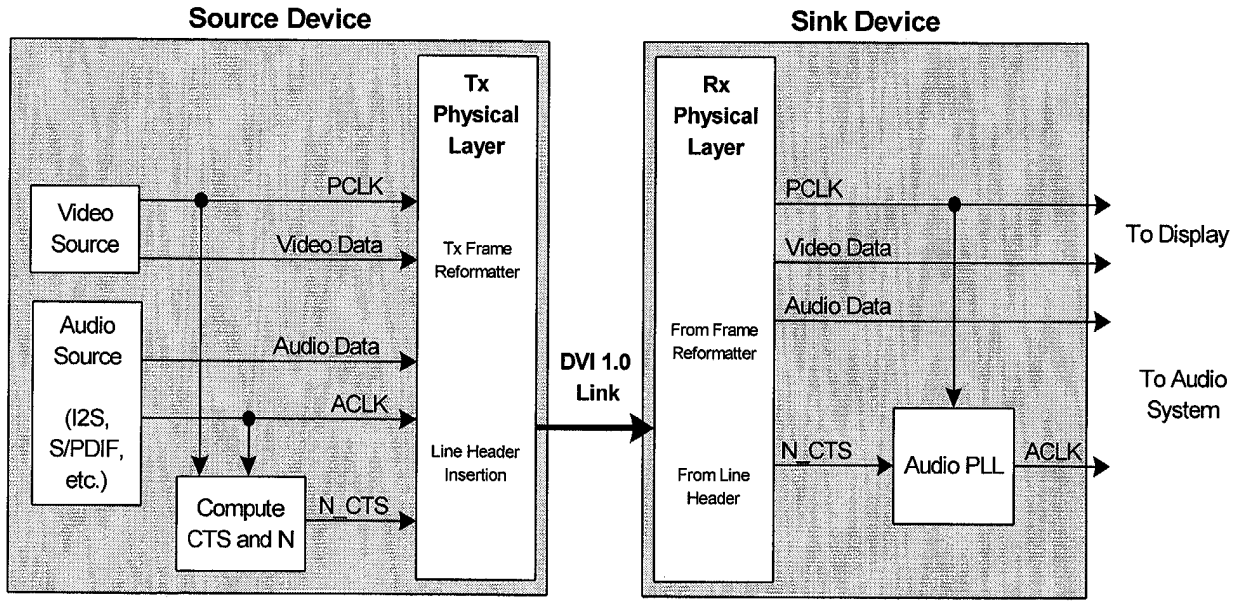

Source Device
Sink Device
Tx Physical Layer
Rx Physical Layer
Video Source
Audio Source
(I2S, S/PDIF, etc.)
PCLK
Video Data
Audio Data
ACLK
N_CTS
Compute CTS and N
Tx Frame Reformatter
Line Header Insertion
DVI 1.0 Link
From Frame Reformatter
From Line Header
Audio PLL
To Display
To Audio System

Fig. 17

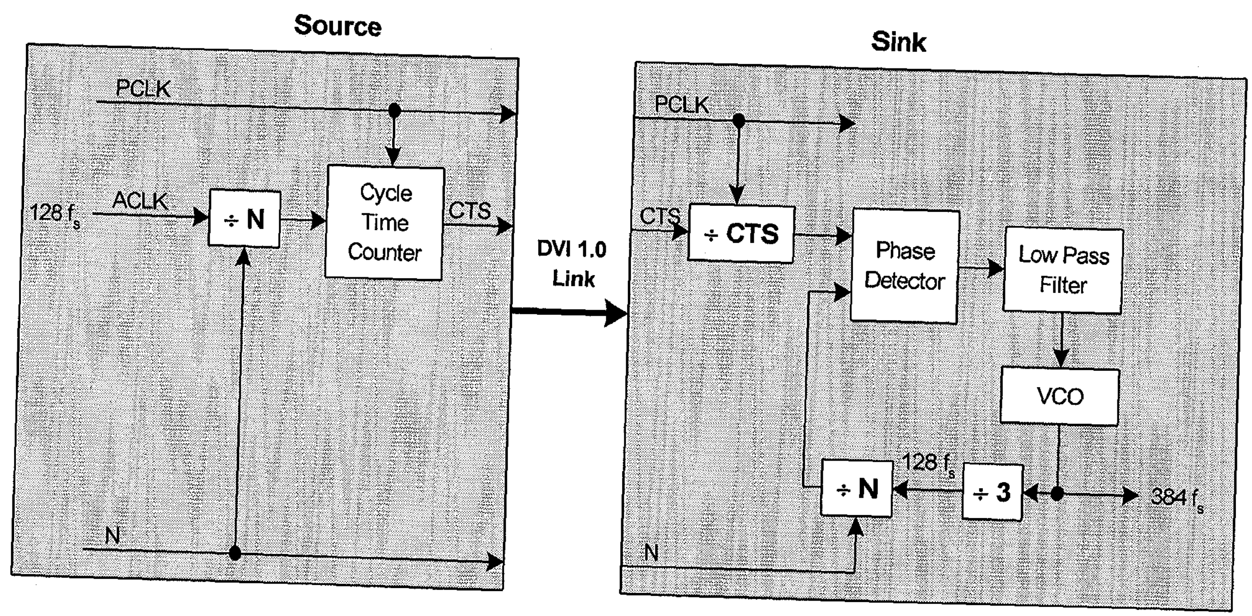

Source
PCLK
128 f_s
ACLK
÷ N
Cycle Time Counter
CTS
N
DVI 1.0 Link
Sink
PCLK
CTS
÷ CTS
Phase Detector
Low Pass Filter
VCO
÷ N
128 f_s
÷ 3
384 f_s
N

Fig. 18

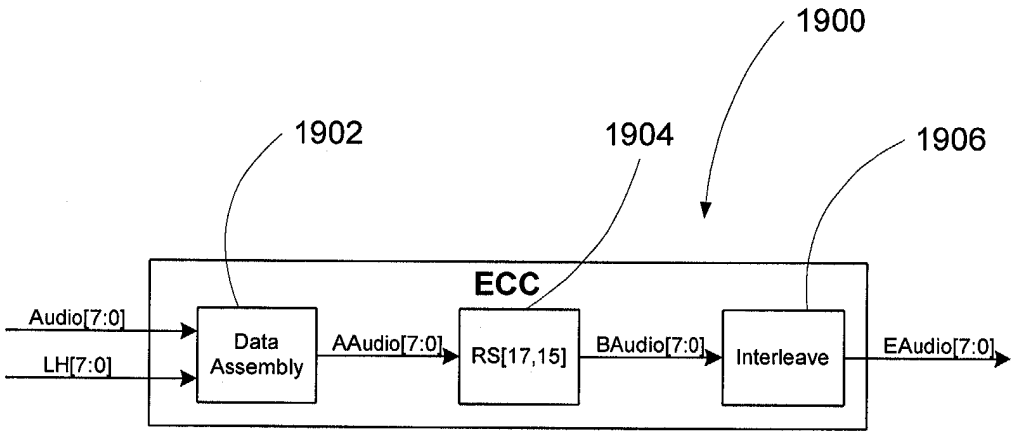

1900
1902
1904
1906
ECC
Audio[7:0]
LH[7:0]
Data Assembly
AAudio[7:0]
RS[17,15]
BAudio[7:0]
Interleave
EAudio[7:0]

Fig. 19

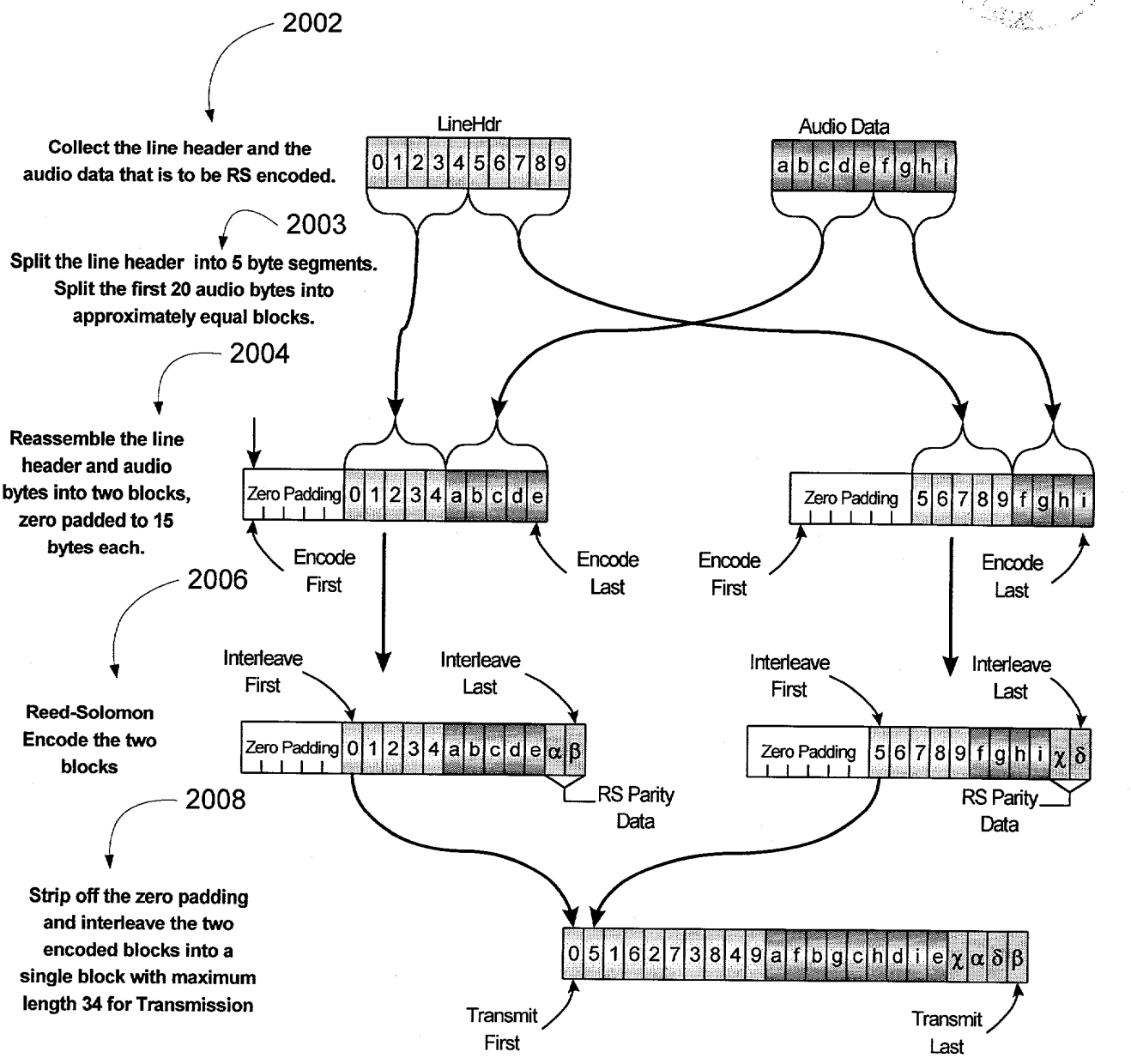

2002
Collect the line header and the audio data that is to be RS encoded.
LineHdr
0 1 2 3 4 5 6 7 8 9
Audio Data
a b c d e f g h i
2003
Split the line header into 5 byte segments. Split the first 20 audio bytes into approximately equal blocks.
2004
Reassemble the line header and audio bytes into two blocks, zero padded to 15 bytes each.
Zero Padding 0 1 2 3 4 a b c d e
Zero Padding 5 6 7 8 9 f g h i
Encode First
Encode Last
Encode First
Encode Last
2006
Reed-Solomon Encode the two blocks
Interleave First
Interleave Last
Interleave First
Interleave Last
Zero Padding 0 1 2 3 4 a b c d e α β
Zero Padding 5 6 7 8 9 f g h i χ δ
RS Parity Data
RS Parity Data
2008
Strip off the zero padding and interleave the two encoded blocks into a single block with maximum length 34 for Transmission
0 5 1 6 2 7 3 8 4 9 a f b g c h d i e χ α δ β
Transmit First
Transmit Last

Fig. 20

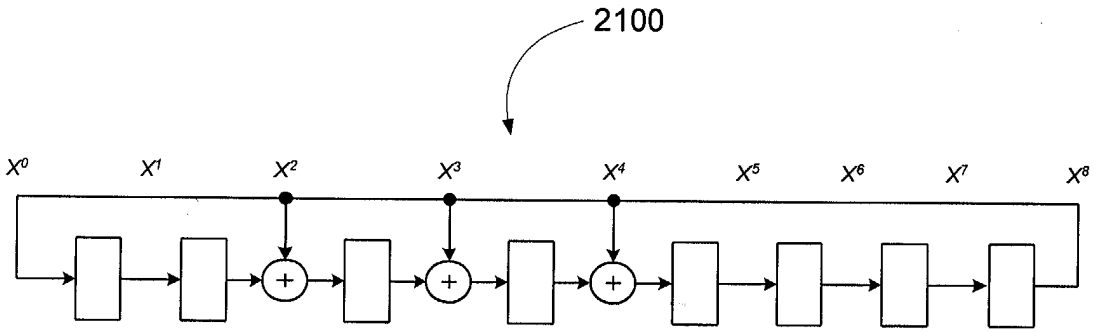


Fig. 21

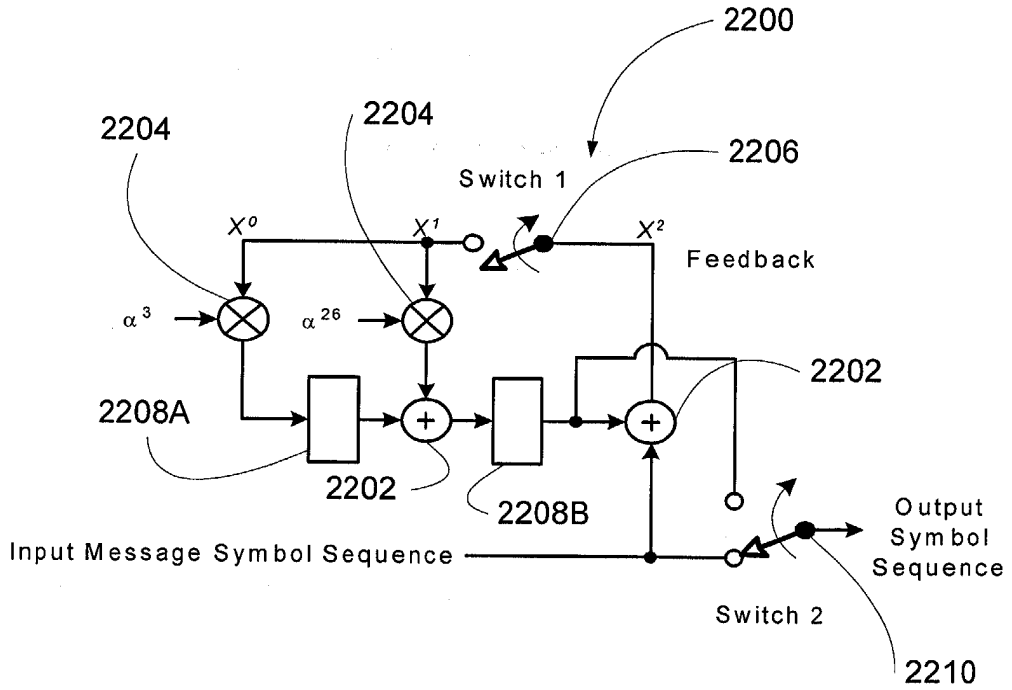


Fig. 22

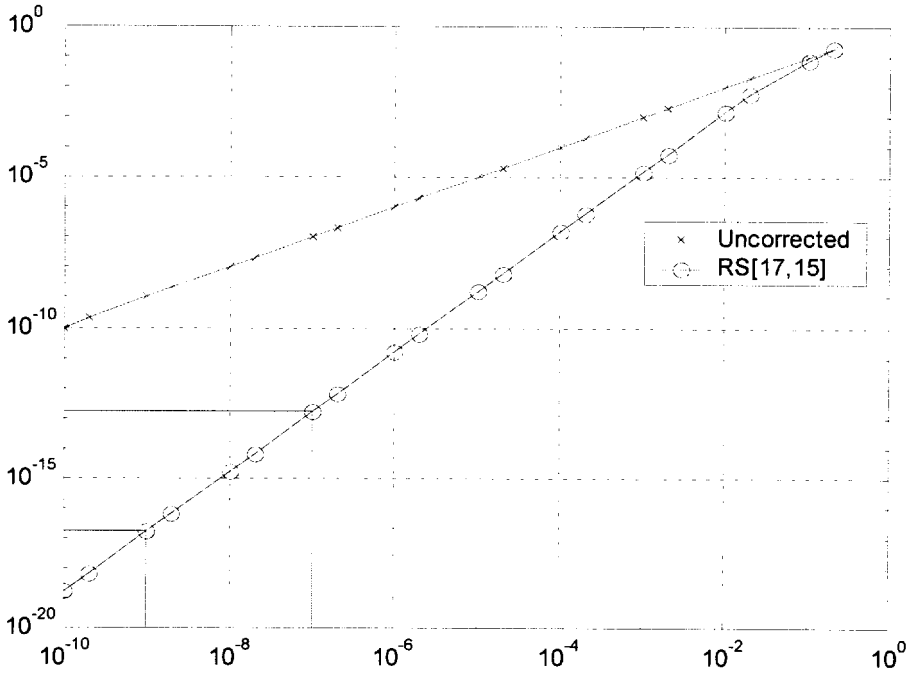

10^{0}
10^{-5}
10^{-10}
10^{-15}
10^{-20}
10^{-10}
10^{-8}
10^{-6}
10^{-4}
10^{-2}
10^{0}
Uncorrected
RS[17,15]

Fig. 23

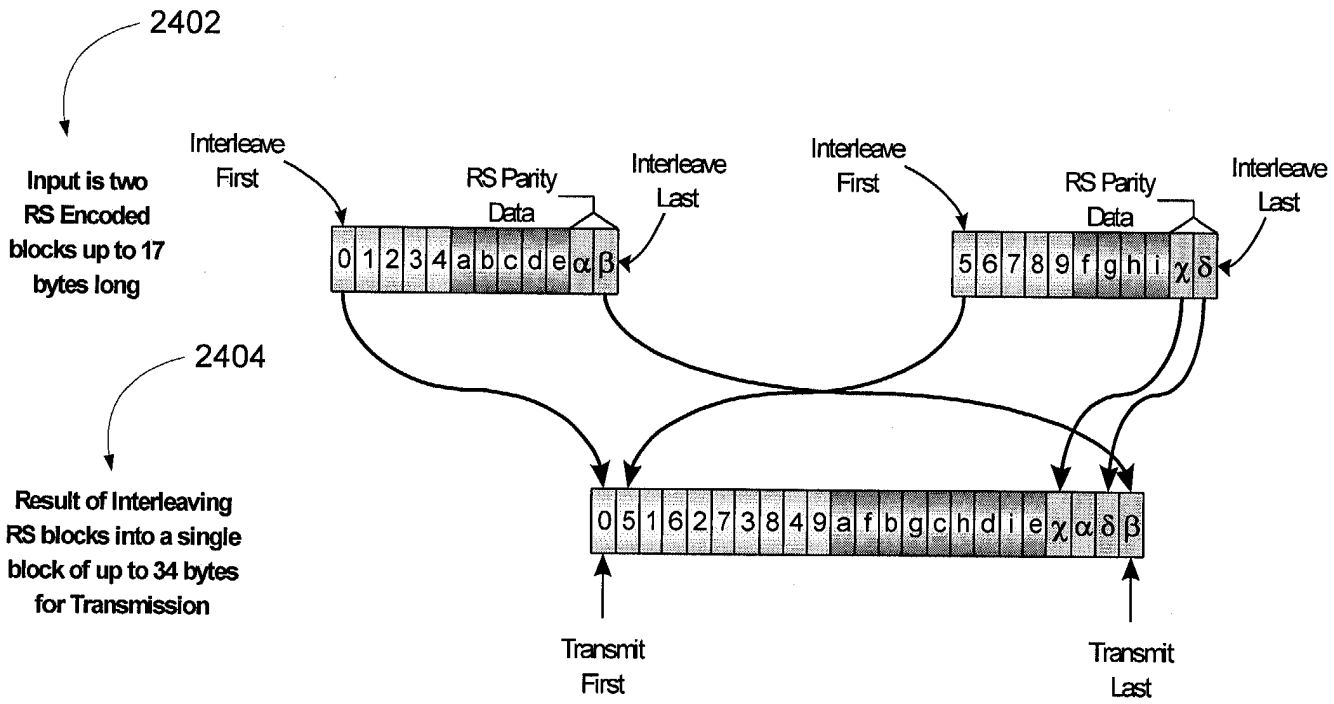

2402
Input is two RS Encoded blocks up to 17 bytes long
Interleave First
RS Parity Data
Interleave Last
0 1 2 3 4 a b c d e α β
Interleave First
RS Parity Data
Interleave Last
5 6 7 8 9 f g h i χ δ
2404
Result of Interleaving RS blocks into a single block of up to 34 bytes for Transmission
0 5 1 6 2 7 3 8 4 9 a f b g c h d i e χ α δ β
Transmit First
Transmit Last

Fig. 24

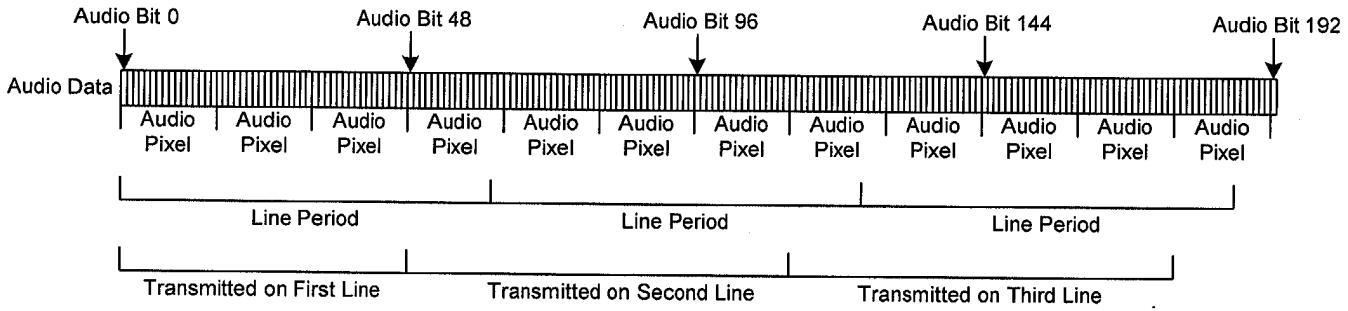

Audio Bit 0
Audio Bit 48
Audio Bit 96
Audio Bit 144
Audio Bit 192
Audio Data
Audio Pixel
Line Period
Line Period
Line Period
Transmitted on First Line
Transmitted on Second Line
Transmitted on Third Line

Fig. 25

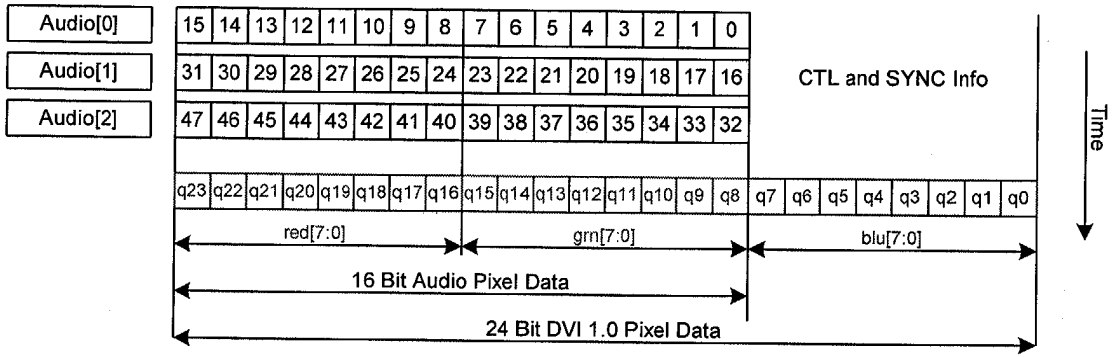

Audio[0]
Audio[1]
Audio[2]
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16
47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32
CTL and SYNC Info
Time
q23 q22 q21 q20 q19 q18 q17 q16 q15 q14 q13 q12 q11 q10 q9 q8 q7 q6 q5 q4 q3 q2 q1 q0
red[7:0]
grn[7:0]
blu[7:0]
16 Bit Audio Pixel Data
24 Bit DVI 1.0 Pixel Data

Fig. 26

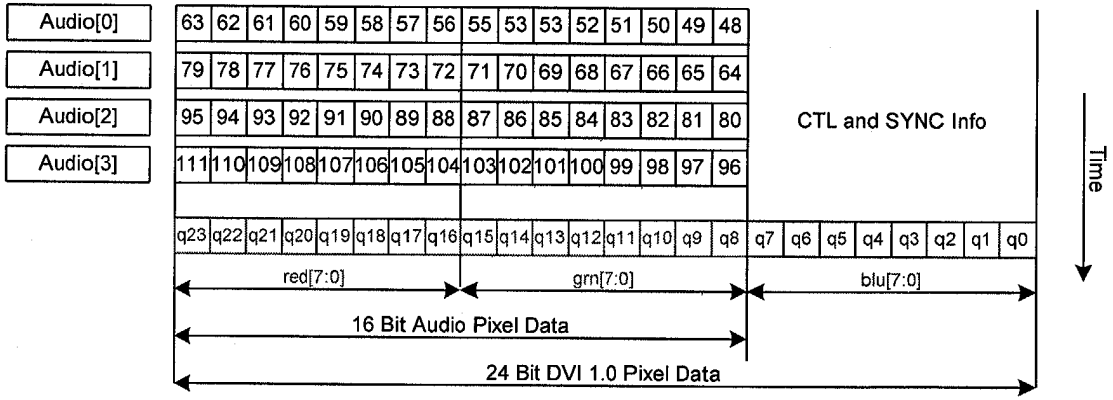

Audio[0]
Audio[1]
Audio[2]
Audio[3]
63 62 61 60 59 58 57 56 55 53 53 52 51 50 49 48
79 78 77 76 75 74 73 72 71 70 69 68 67 66 65 64
95 94 93 92 91 90 89 88 87 86 85 84 83 82 81 80
111 110 109 108 107 106 105 104 103 102 101 100 99 98 97 96
CTL and SYNC Info
q23 q22 q21 q20 q19 q18 q17 q16 q15 q14 q13 q12 q11 q10 q9 q8 q7 q6 q5 q4 q3 q2 q1 q0
red[7:0]
grn[7:0]
blu[7:0]
16 Bit Audio Pixel Data
24 Bit DVI 1.0 Pixel Data
Time

Fig. 27

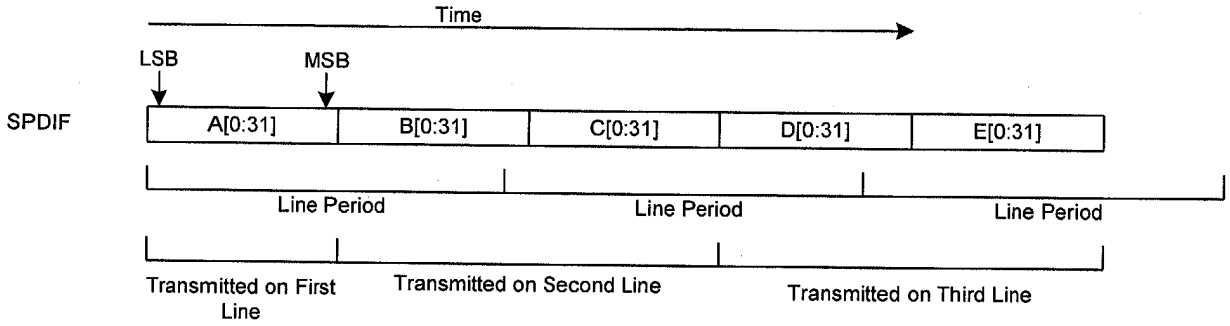

Time
LSB
MSB
SPDIF
A[0:31]
B[0:31]
C[0:31]
D[0:31]
E[0:31]
Line Period
Line Period
Line Period
Transmitted on First Line
Transmitted on Second Line
Transmitted on Third Line

Fig. 28

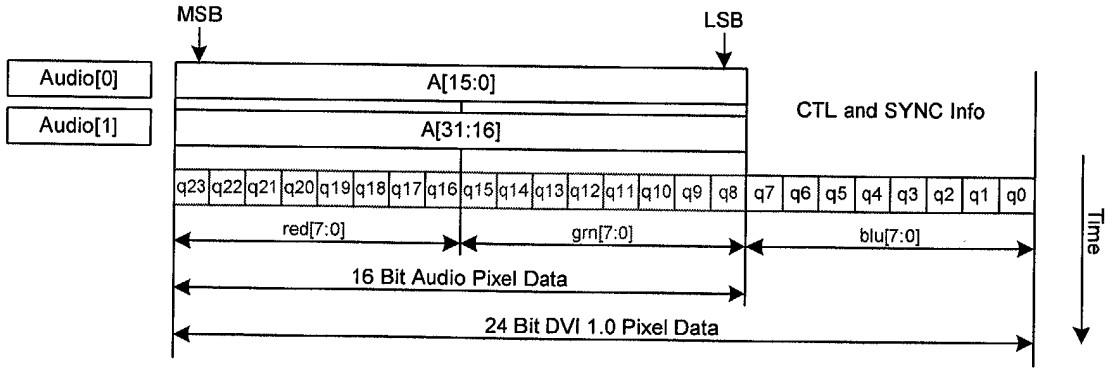

MSB
LSB
Audio[0]
Audio[1]
A[15:0]
A[31:16]
CTL and SYNC Info
q23 q22 q21 q20 q19 q18 q17 q16 q15 q14 q13 q12 q11 q10 q9 q8 q7 q6 q5 q4 q3 q2 q1 q0
red[7:0]
grn[7:0]
blu[7:0]
16 Bit Audio Pixel Data
24 Bit DVI 1.0 Pixel Data
Time

Fig. 29

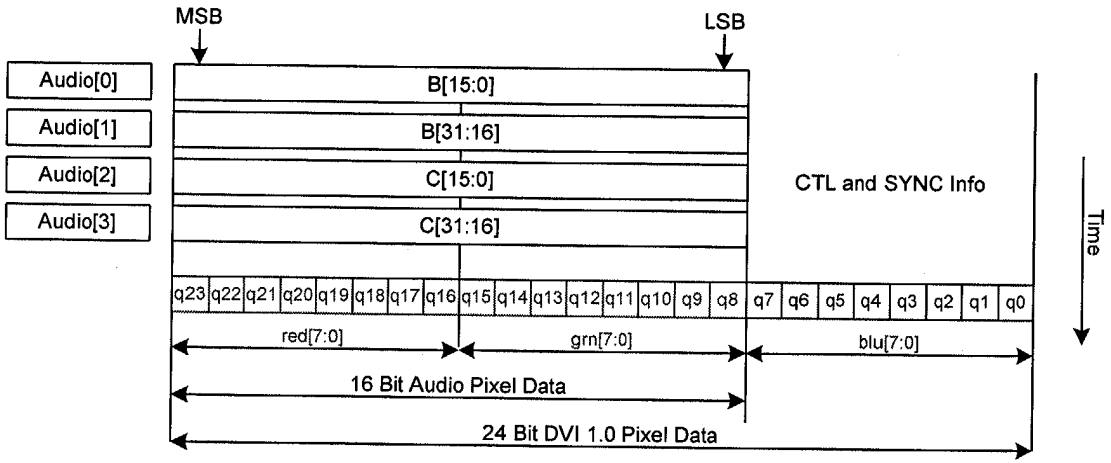


Fig. 30

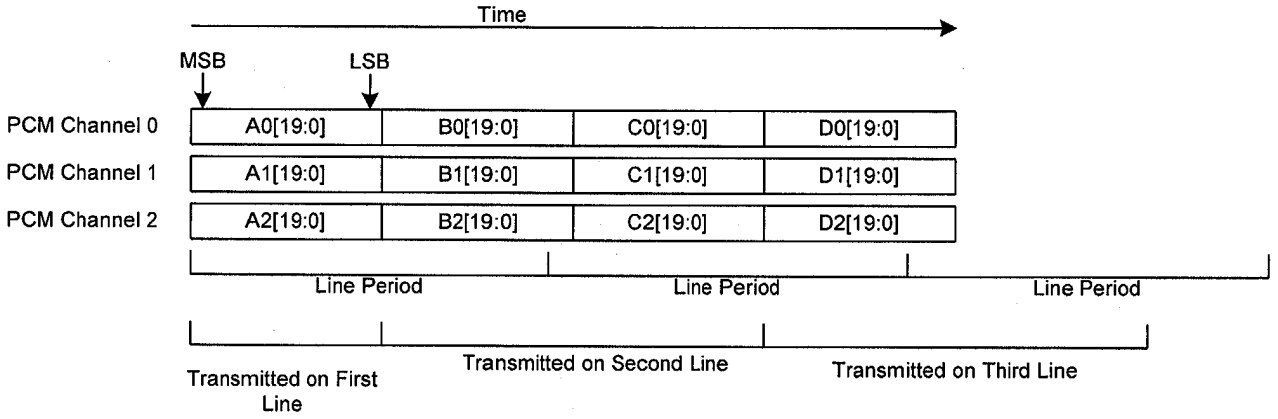

Time
MSB
LSB
PCM Channel 0
PCM Channel 1
PCM Channel 2
A0[19:0]
B0[19:0]
C0[19:0]
D0[19:0]
A1[19:0]
B1[19:0]
C1[19:0]
D1[19:0]
A2[19:0]
B2[19:0]
C2[19:0]
D2[19:0]
Line Period
Line Period
Line Period
Transmitted on First Line
Transmitted on Second Line
Transmitted on Third Line

Fig. 31

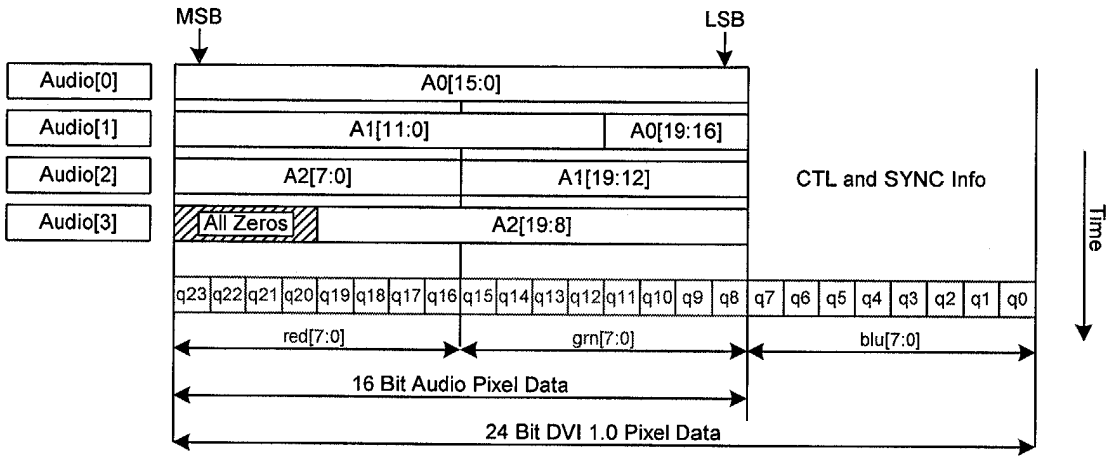

MSB
LSB
Audio[0]
Audio[1]
Audio[2]
Audio[3]
A0[15:0]
A1[11:0]
A0[19:16]
A2[7:0]
A1[19:12]
All Zeros
A2[19:8]
CTL and SYNC Info
Time
q23 q22 q21 q20 q19 q18 q17 q16 q15 q14 q13 q12 q11 q10 q9 q8 q7 q6 q5 q4 q3 q2 q1 q0
red[7:0]
grn[7:0]
blu[7:0]
16 Bit Audio Pixel Data
24 Bit DVI 1.0 Pixel Data

Fig. 32

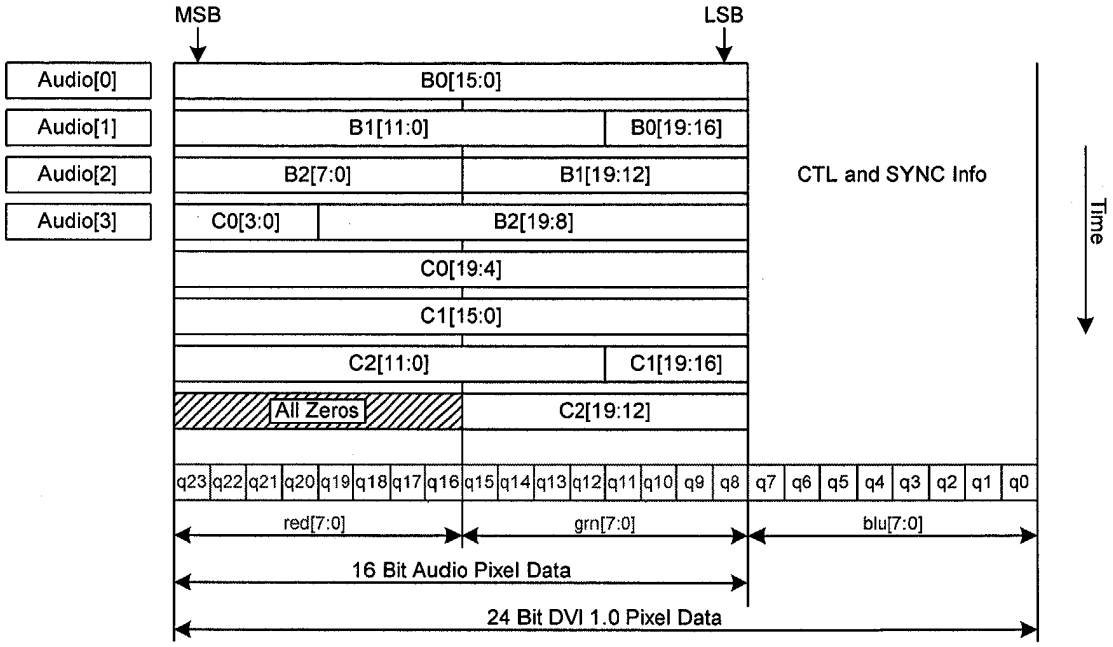

MSB
LSB
Audio[0]
Audio[1]
Audio[2]
Audio[3]
B0[15:0]
B1[11:0]
B0[19:16]
B2[7:0]
B1[19:12]
C0[3:0]
B2[19:8]
C0[19:4]
C1[15:0]
C2[11:0]
C1[19:16]
All Zeros
C2[19:12]
CTL and SYNC Info
Time
q23 q22 q21 q20 q19 q18 q17 q16 q15 q14 q13 q12 q11 q10 q9 q8 q7 q6 q5 q4 q3 q2 q1 q0
red[7:0]
grn[7:0]
blu[7:0]
16 Bit Audio Pixel Data
24 Bit DVI 1.0 Pixel Data

Fig. 33